A Technique to Reduce the Capacitor size in Two Stage Miller compensated opamp.

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***Abstract*— In this paper two stage Miller compensated opamp has been discussed qualitatively and quantitatively. A modification to the conventional compensation network has been proposed, which will reduce the capacitor size hence circuit area. Transfer function for the newly proposed solution has been derived and explained the results. A prototype was developed in 65nm TSMC CMOS technology and simulation results have been presented. Amplifier achieved 60dB low frequency gain, 12MHz bandwidth and 55^0 phase margin while consuming 650uW power from 1.2V power supply. Circuit occupies 5348um ^{2}silicon area.**

Keywords—Opamp, phase margin, Stability, CMFB, Compensation, capacitor, Scaling.

I. INTRODUCTION

The recent advancement in the CMOS scaling developed the road for the growing market of advanced electronics applications in mobiles, sensor applications. The scaling is driven by the integration of complex features on the same chip (like SOC) with continuous improvement in the operating speed and decrement in the system power consumption [1]. The CMOS scaling is very much encouraged from digital designers because of the decrease in the switching power (CV^2F), but it creates a lot of troubles to analog design based systems. The operational trans-conductance amplifier (OTA) provides an easy way of creating negative feedback for providing accurate bias voltage due to their high voltage gain which enables system performance robust against Process, Voltage, Temperature(PVT) corners. With the scaling, the power supply voltage is dropping to maintain the constant electric field in the transistors, but the threshold voltage of the transistor is not dropping in the same pace, hence transistors in the opamps are not getting enough over-driver voltages(Vd_{SAT}) to provide reasonable voltage gain[2]. Fig:1 show how the voltages are dropping for different technology generations. At 65nm CMOS node, maximum V_{dd} is ~1V but V_{th} is 0.35V. Fig:2 shows the simulated gain of a single stage opamp across different technologies, at 65nm node, maximum achievable gain ~28dB, which is much lesser than acceptable gain for any application. For a feedback loop to produce 0.1% accuracy, loop-gain must be much higher than 60dB. Cascode opamps can potentially produce much higher voltage gain, but limited available supply V_{dd} limits the number of devices can be stacked [3].

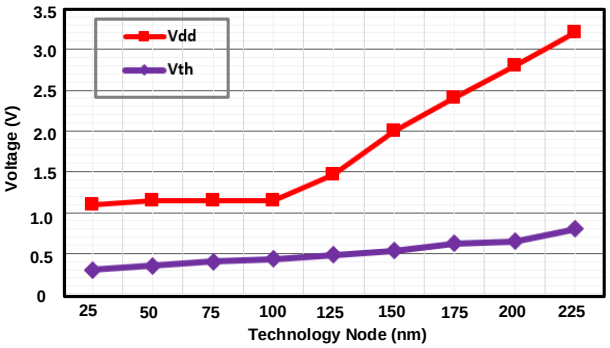

Fig. 1. Leakage current versus Technology Node

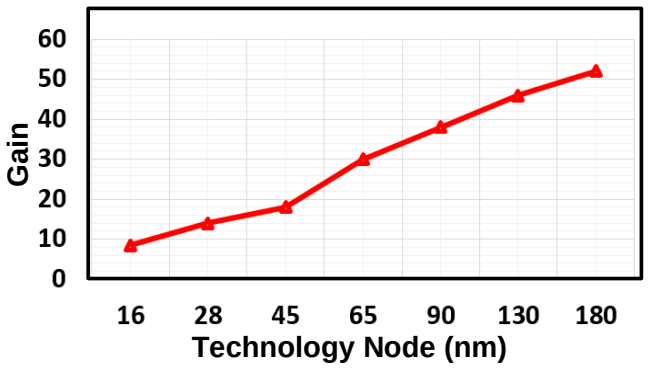

Fig. 2. Single stage opamp gain versus Technology Node

Gain boosting technique will always achieve gain >80dB but it requires nested opamp along with compensation requirement and closed space pole-zero double could lead to slow settling step response [4]. Hence the practical gain requirement calls for multistage opamp techniques in deep sub-micron CMOS technology-based designs.

Multi-stage amplifier technique known for several decades and there has been a lot of research, which achieved >140dB gain. Cascading several stages leads to several closely spaced poles which could degrades the stability of the opamps. To combat with the stability, frequency compensation must be done, to ensure well-behaved transient step response. Widely known techniques are miller, cascode, Ahuja compensations. Miller compensation known for its bandwidth enhancement through pole splitting

phenomena. In the past, although various miller compensation schemes have been proposed to improve the gain bandwidth product, complexity also increased interims of additional amplifier stages and capacitors. Miller compensation with a nulling resistor introduces a right half zero (RHP) which compromises the stability. Ahuja [5] proposed a current buffer in series with a compensation capacitor to cancel RHP, downside of this technique is complex poles in the closed loop. Ribner [6] has proposed cascade compensation, by connection compensation capacitor at low impedance node to eliminate RHP zero, often creating a low impedance node with-in the Opamp demands a lot of power. A damping stage based compensation proposed in [7][11], but the technique has poor power supply rejection (PSRR). This paper proposes a technique to reduce the compensation capacitor for a given phase margin, hence reduced circuit area as well power dissipation.

The paper has been organized as follows, section-2 deals with the well-known miller compensation intuitively and derives relevant equations. Section-3 describes the proposed technique and section-4 summarizes the proto type results.

II. TWO STAGE OPAMP MILLER COMPENSATION.

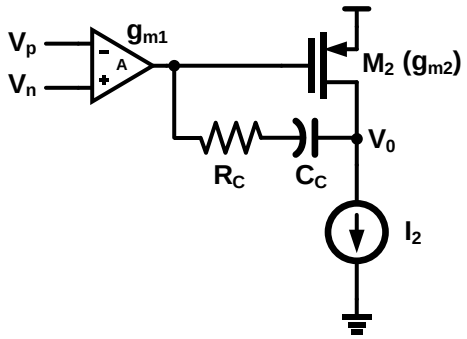

Fig. 3. Traditonal miller compensated opamp.

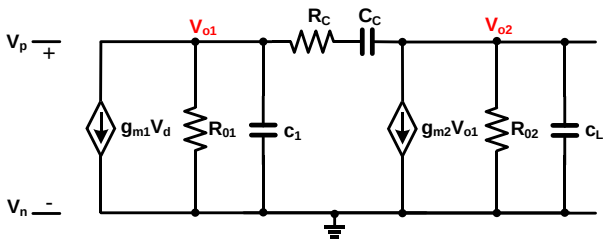

Fig. 4. Traditonal miller compensated opamp.

Fig. 2 depicts the standard two stage miller compensated operational amplifier, where the first stage is a differential amplifier with current source load, whereas second stage is single ended common source amplifier. First and second stage trans-conductance, output impedance and capacitance represented as g_{m1},R_{01},C_1,g_{m2},R_{02},C_L. Two poles of the amplifier are located at $1/R_{o1}*C_1$ and $1/R_{o2}*C_{L,}$ to ensure stability, these two pole frequencies should far enough, hence a compensation series network has been added to split the poles. Fig:4 shows the small signal model of the two stage opamp and voltage gain transfer function can be expressed as follows.

$$\frac{V_o(S)}{V_{in}(S)} = \frac{g_{m1}g_{m2}}{g_{01}g_{02}} \frac{B_1S+1}{A_3S^3+A_2S^2+A_1S+1} \qquad (1)$$

Where $B_1 = C_C(R_C - \frac{1}{g_{m2}})$

$$A_3 = \frac{C_C C_{01} C_L R_C}{g_{01}g_{02}}$$

$$A_2 = \frac{R_C C_C(g_{01}C_L+g_{02}C_{01})+C_L C_{01}+C_L C_C+C_C C_{01}}{g_{01}g_{02}}$$

$$A_1 = \frac{C_L g_{01}+C_{01}g_{02}+(g_{m2}+g_{01}+g_{02}+g_{01}g_{02}R_C)C_C}{g_{01}g_{02}}$$

Using wide pole approximation poles of the transfer function poles can be expressed as

$$P_1 = \frac{g_{01}}{C_1+C_C\frac{g_{m2}}{g_{02}}} \quad \text{and} \quad P_2 = \frac{g_{m2}\frac{C_C}{C_C+C_1}}{C_L+\frac{C_1C_C}{C_1+C_C}} \sim \frac{g_{m2}}{C_L}$$

From the above approximated pole locations we can conclude P_1 is much lesser than initial position ($1/R_{o1}*C_1$), because of the miller multiplication C_C will be magnified by the second stage gain (g_{m2}/g_{ds2}).

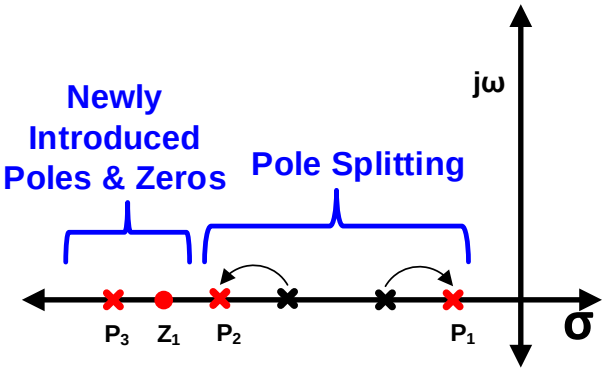

Fig. 5. Traditonal miller compensated opamp.

Non-dominate pole P_2 will be much larger than the initial position ($1/R_{o2}*C_L$), because the second stage transistor (M_2) behaves like diode connected load which presents very low impedance$1/g_{m2}$. Hence dominate pole becomes more dominant and non-dominate pole moves to very high frequency, this is called pole-splitting. Unfortunately, C_C not only acts like feedback element, also feedforward signal from first stage to second stage which creates right half zero (RHZ) in the transfer function hence leads to phase margin degradation due to the additional phase lead. To block the feedforward, signal a resistance will be used in series with capacitor which will move the RHP to high frequency sometimes even to left half to add phase lead (which will improve the phase margin). [5] used a current buffer and [8] used a voltage buffer to push the zero frequency, but often this consumes significant power so chosen series resistor in this work. R_c will introduce another pole (without R_c system is 2nd order and with R_c 3rd order), this pole frequency must be much higher than second dominate pole, hence there will be a maximum value on this. Fig:5 shows the pole splitting

phenomena and newly introduced high frequency poles and zeros graphically. The disadvantage of miller compensation is for a given load capacitance is it requires much higher capacitance to maintain the reasonable phase margin (60^0) because the second dominate pole (P_2) strongly depends on the load capacitance and hence C_C also depends on the load capacitance [10].

$$PM = 90^0 - \tan^{-1}\left(\frac{g_{m1}}{g_{m2}}\frac{C_L}{C_C}\right) \quad (2)$$

III. PROPOSED TECHNIQUE.

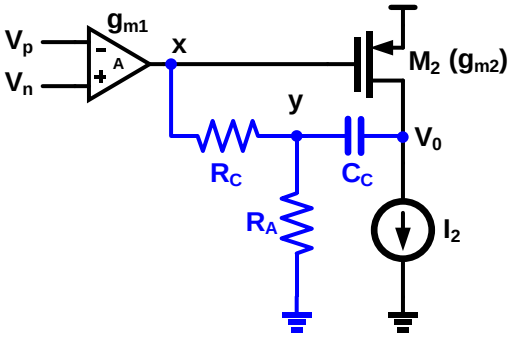

Fig. 6. Proposed compensation technique

Fig:6 shows the proposed compensation strategy, fundamentally introduced a high frequency current leaky path has been introduced in the traditional compensation network. At low frequencies, R_a impedance is much higher than c_c impedance hence there is no feedback like the traditional miller compensation. At high frequency CC impedance is much lower than Ra hence there is a feedback through capacitor but Ra keep drawing some signal current, such that current flowing into the node x is always lesser than the traditional compensation. This is like having much higher capacitance than what it was presented in the schematic. A pole zero analysis of the proposed amplifier revels that it is a 3rd order system like miller technique but there has been two zero (means one zero higher than existing tech) frequencies. Important point to note is unity gain bandwidth (UGB) of the amplifier is not only depends on gm1 of the first stage but also R_A, as expressed as (3).

$$W_{ugb} \sim \frac{1}{C_C\left(R_A + \frac{1}{gm}\frac{R_A}{R_C}\right)} \quad (3)$$

If first stage g_m is very high then UGB depends only on C_C,R_A.

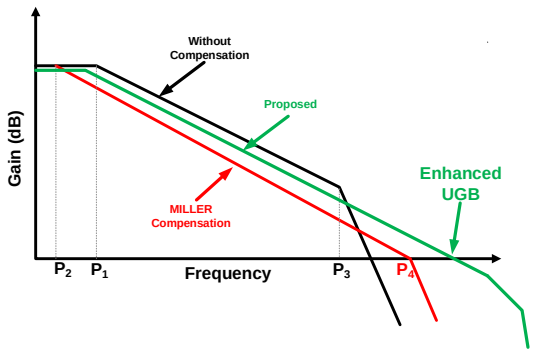

Fig. 7. Graphical comparion of the existed and proposed technique

A little concern with the miller technique is miler capacitance CC decides the integrated thermal noise, whereas in the proposed it will be attenuated by R_A because of the current shunting reason. Fig:7 shows the graphical illustration of how the presented compensation improves the UGB compared to the existing one for a given g_{m1}.Little down of this technique is a very minor reduction in the dc gain due to compensation network loading and there has been new high frequency pole has been introduced, which needs to place carefully otherwise it may compromise the stability.

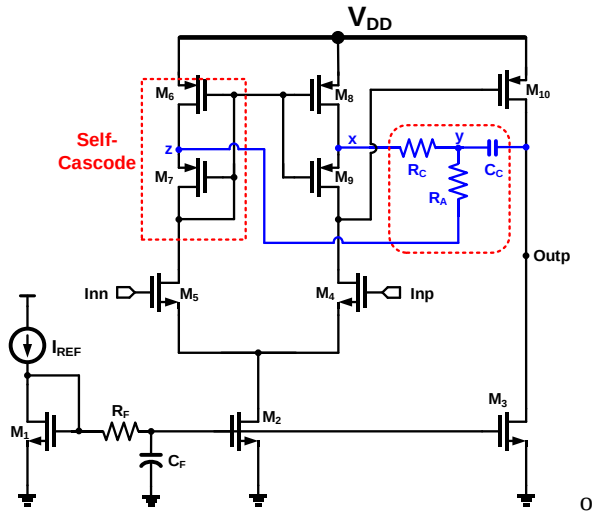

Fig. 8. Implementation of Proposed compensation technique

Fig. 8 depicts the transistor level implementation of the presented technique, first stage is nmos input differential pair with self Cascode pmos current source load. As explain in [8], connecting compensation network to a low impedance point will results in high frequency RHP and helps stability, hence self Cascode create low impedance nodes x,z without costing any power. Another requirement for low impedance node is in fig. 6 R_A connected to a ac ground, not the DC ground hence R_A has been terminated to node Z, in this way compensation network loading on the first stage also reduced to some extent.

IV. SIMULATION RESULTS

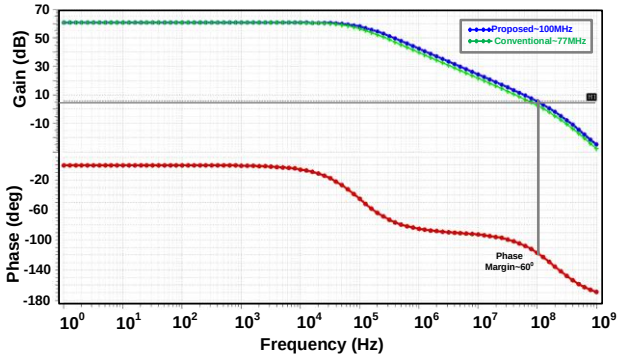

Fig. 9. Frequency Response of the Prposed technique

Proposed technique has been implemented in 65nm CMOS TSMC technology and post layout simulation results as follows. , fig. 9 shows the frequency response of the proposed amplifier depicts 100MHz UGB, where for the same power consumption existing miller technique has 77MHz only (~29% improvement). Fig:10 shows the large signal DC transfer characteristics of the amplifier, slope of the curve around 0mV differential voltage is ~1000, confirms 60dB gain from ac response.

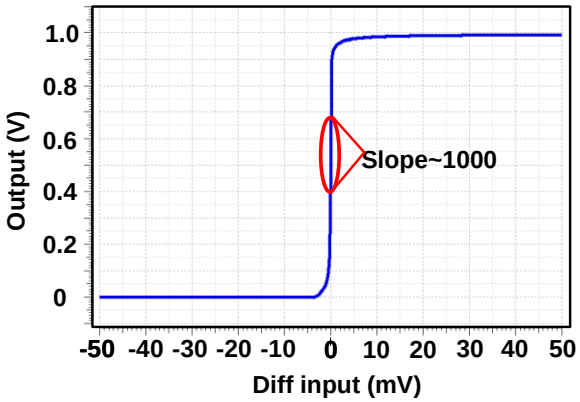

Fig. 10. DC characteristics of the opamp

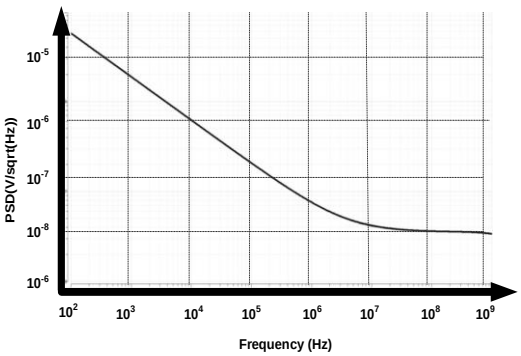

Fig. 11. Input referred spectral density of the opamp

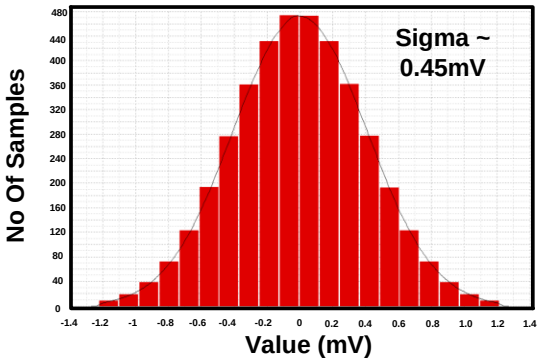

Fig. 12. Input referred spectral density of the opamp

Fig. 11 depicts the input referred noise, integrated spectral density results in 0.2uV RMS noise. Fig. 12 shows the input referred noise, 1000 MC shows 1-sigma of 0.42mV. Fig. 13 depicts the layout of the amplifier, occupies 4160um^2 silicon area. Circuit draws 180uA current from 1V power supply.

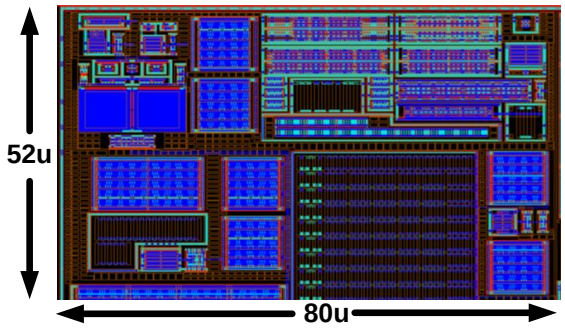

Fig. 13. Layout of the proposed Solution.

V. Conclusion

In this paper, modified miller compensation has been proposed and simulation has been shown to demonstrate the robustness of the technique. 29% improvement has been achieved in UGB of the amplifier while consuming same power.

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